

Remarks

Reconsideration of this application as amended is respectfully requested.

Claims 1, 2, 5, 11, 12, and 15 stand rejected under 35 U.S.C. §102(b) in view of JP5-22048.

Claims 3, 4, 6, 13, 14 and 16 stand rejected under 35 U.S.C. §103(a) in view of a publication in Japanese JP5-22048.

The examiner has stated that claims 7-10 and 17-20 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In response, applicant has amended claim 7 to include all of the limitations of base claim 1 and has amended claim 17 to include all of the limitations of base claim 11. Given that claims 8-10 and 18-20 depend from amended claims 7 and 10, respectively, it is submitted that claims 7-10 and 17-20 are in a condition for allowance.

Applicant submits that claim 1 is not anticipated by JP5-22048 because the content of that publication that is readable in English does not disclose a two stage amplifier including a first amplifier stage and a second amplifier stage and a pair of components coupled in series between the first and second amplifier stages that are selected to provide AC decoupling between the first and second amplifier stages and stability in the two stage amplifier. The examiner has stated that Figure 1 of JP5-22048 discloses a component L3 that is selected to provide AC decoupling of a first amplifier stage 3 and a second amplifier stage 4 and a component R1 that is selected to provide for stability of the first and second amplifier stages 3 and 4 (Page 2, Office Action, 10-7-05) but has not cited any language in JP5-22048 in support. Figure 1 of JP5-22048 was cited by the examiner but Figure 1 of JP5-22048 does not indicate that the

component L3 is selected to provide AC decoupling or that the component R1 is selected to provide for stability. Instead, Figure 1 of JP5-22048 shows only electrical circuit symbols and references to those symbols.

It is further submitted that transistors 3 and 4 in Figure 1 of JP5-22048 are not a first and second amplifier stage as stated by the examiner. Instead, Figure 1 of JP5-22048 discloses a first differential amplifier stage made up of transistors 1 and 2 and a second differential amplifier stage made up of transistors 3 and 4. For example, transistors 1 and 2 in Figure 1 of JP5-22048 both receive a signal 5, possibly an input signal, and transistors 3 and 4 in Figure 1 of JP5-22048 both drive a load R_L , possibly an output load. Figure 1 of JP5-22048 does not disclose a pair of components coupled in series between the first (1,2) and second (3,4) differential amplifier stages that are selected to provide AC decoupling and stability as does a two-stage amplifier according to claim 1.

Given that claims 2-6 depend from claim 1, it is submitted that claims 2-6 are not anticipated by JP5-22048.

It is also submitted that claim 11 is not anticipated by JP5-22048. Claim 11 includes limitations similar to the limitations of claim 1. Therefore, the remarks stated above with respect to claim 1 and JP5-22048 also apply to claim 11.

Given that claims 12-16 depend from claim 11, it is submitted that claims 12-16 are not anticipated by JP5-22048.

It is further submitted that claims 3, 4, 6, 13, 14 and 16 are not obvious in view of JP5-22048. Claims 3, 4, 6, 13, 14 and 16 depend from claims 1 and 11 and JP5-22048 does not disclose or suggest a first and a second component coupled in series between the first and second


amplifier stages of a two stage amplifier as claimed in claims 1 and 11 as shown above.

It is respectfully submitted that in view of the amendments and arguments set forth above, the applicable objections and rejections have been overcome.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 50-3718 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

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